HF/VHF power MOS transistor

BLF177

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for industrial and military applications in the HF/VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT121 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the 'General' section for further information.

PIN CONFIGURATION

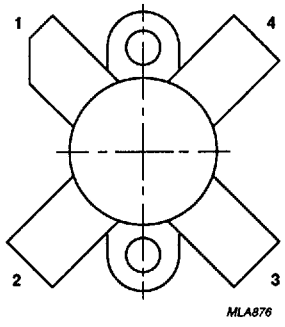


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

PINNING - SOT121

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)	d_5 (dB)
SSB class-AB	28	50	150 (PEP)	> 20	> 35	< −30	< −30
CW class-B	108	50	150	typ. 19	typ. 70	–	–

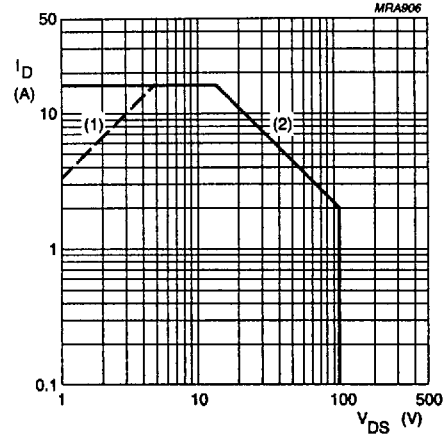
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	110	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	16	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	220	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

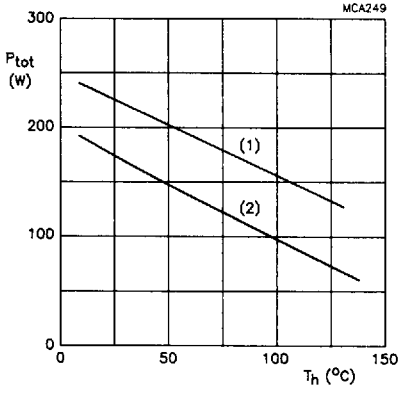
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	max. 0.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	max. 0.2 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



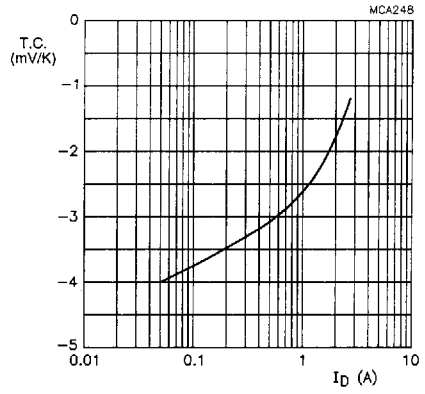
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

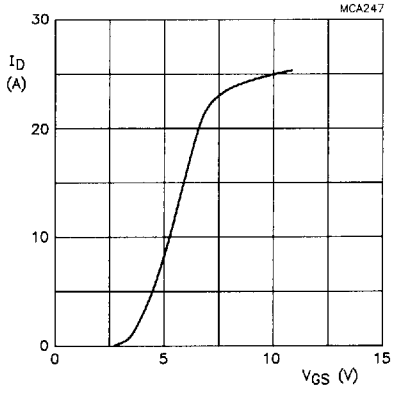
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 50 mA; V_{GS} = 0	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	µA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 5 A; V_{DS} = 10 V	4.5	6.2	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF



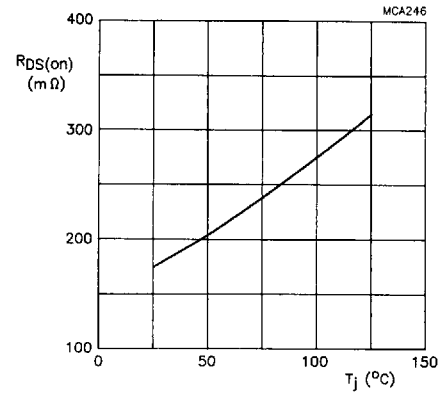
V_{DS} = 10 V; valid for T_h = 25 to 70 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



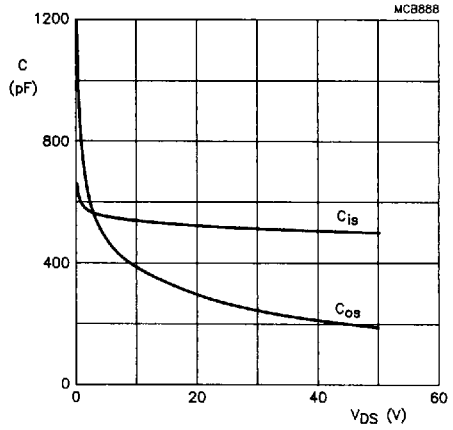
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



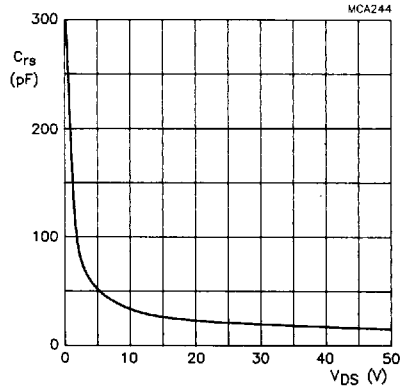
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; Z_L = 6.25 + j0 Ω unless otherwise specified.
RF performance in SSB operation in a common source class-AB circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB) (note 1)	d_5 (dB) (note 1)
SSB, class-AB	28	50	0.7	20 to 150 (PEP)	> 20 typ. 35	> 35 typ. 40	< −30 typ. −35	< −30 typ. −38

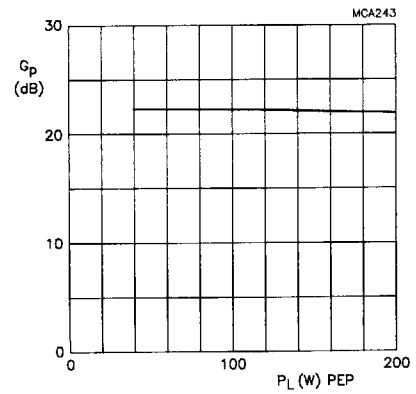
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.

Ruggedness in class-AB operation

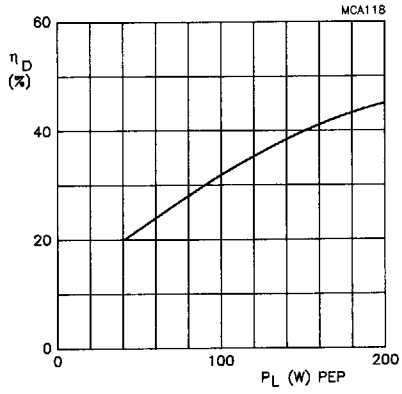
The BLF177 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 50 V; f = 28 MHz at rated output power.



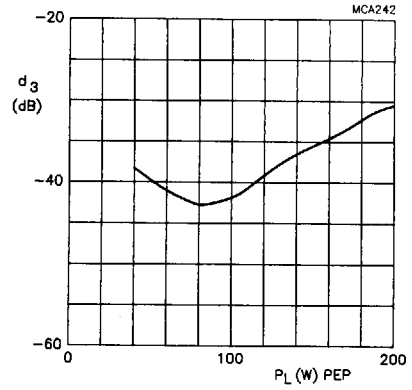
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A; R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.9 Power gain as a function of load power, typical values.



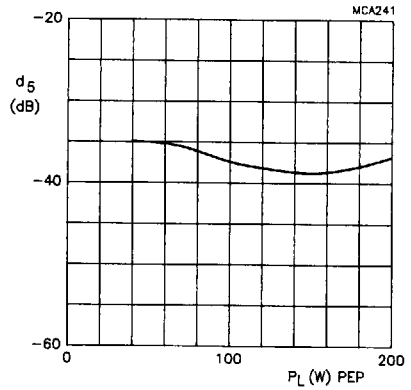
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A; R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.10 Two tone efficiency as a function of load power, typical values.



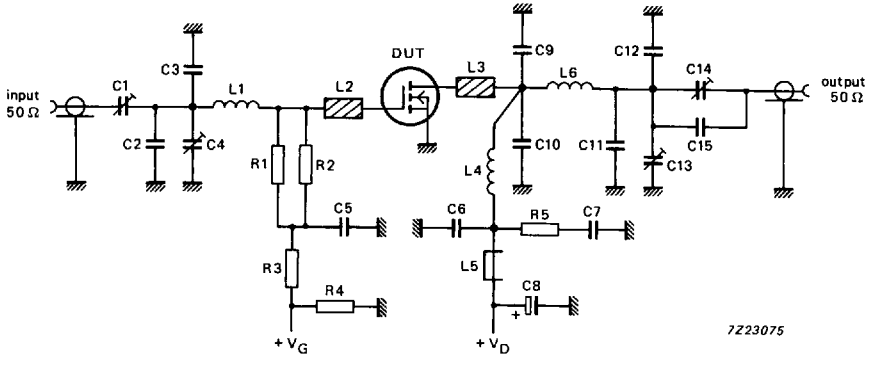
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A; R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.11 Third order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A; R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.12 Fifth order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

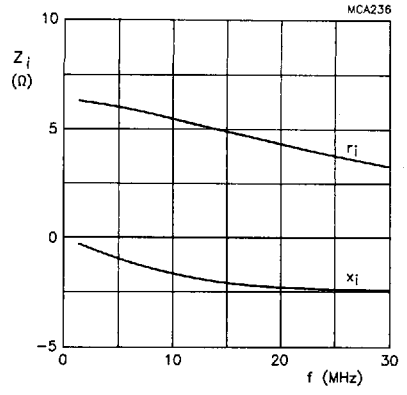
Fig.13 Test circuit for class-AB operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C4, C13, C14	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2	multilayer ceramic chip capacitor (note 1)	56 pF		
C3, C11	multilayer ceramic chip capacitor (note 1)	62 pF		
C5, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C7	multilayer ceramic chip capacitor	3 x 100 nF		2222 852 47104
C5	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C7	multilayer ceramic chip capacitor	3 x 100 nF		2222 852.47104
C8	electrolytic capacitor	2.2 µF, 63 V		
C9, C10	multilayer ceramic chip capacitor (note 1)	20 pF		
C12	multilayer ceramic chip capacitor (note 1)	100 pF		
C15	multilayer ceramic chip capacitor (note 1)	150 pF		
L1	5 turns enamelled 0.7 mm copper wire	133 nH	length 4.5 mm; int. dia. 6 mm; leads 2 x 5 mm	
L2, L3	stripline (note 2)	41.1 Ω	length 13 x 6 mm	
L4	7 turns enamelled 1.5 mm copper wire	236 nH	length 12.5 mm; int. dia. 8 mm; leads 2 x 5 mm	
L5	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L6	5 turns enamelled 2 mm copper wire	170 nH	length 11.5 mm; int. dia. 8 mm; leads 2 x 5 mm	
R1, R2	1 W metal film resistor	10 Ω		
R2	0.4 W metal film resistor	10 kΩ		
R3	0.4 W metal film resistor	1 MΩ		
R5	1 W metal film resistor	10 kΩ		

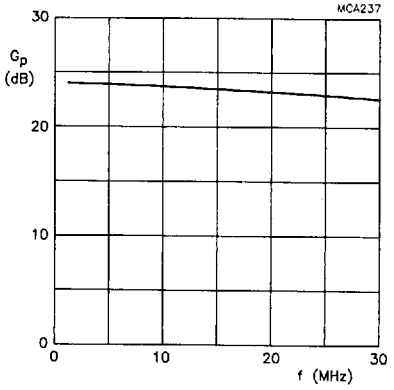
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$), thickness 1.6 mm.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A; P_L = 150 W (PEP); R_{GS} = 6.25 Ω; R_L = 6.25 Ω.

Fig.14 Input impedance as a function of frequency (series components), typical values.



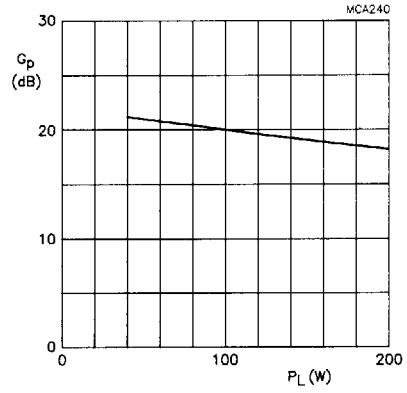
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A; P_L = 150 W (PEP); R_{GS} = 6.25 Ω; R_L = 6.25 Ω.

Fig.15 Power gain as a function of frequency, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

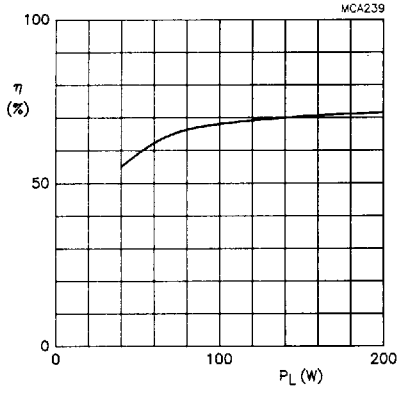
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; R_{GS} = 15.8 Ω; unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	0.1	150	typ. 19	typ. 70



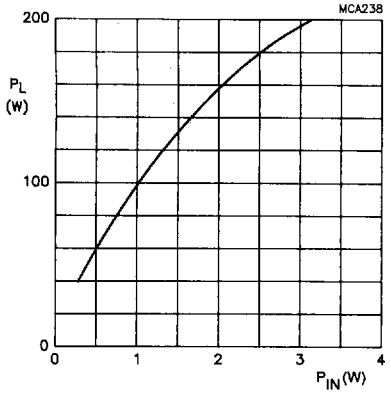
Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 mA; R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.16 Power gain as a function of load power, typical values.



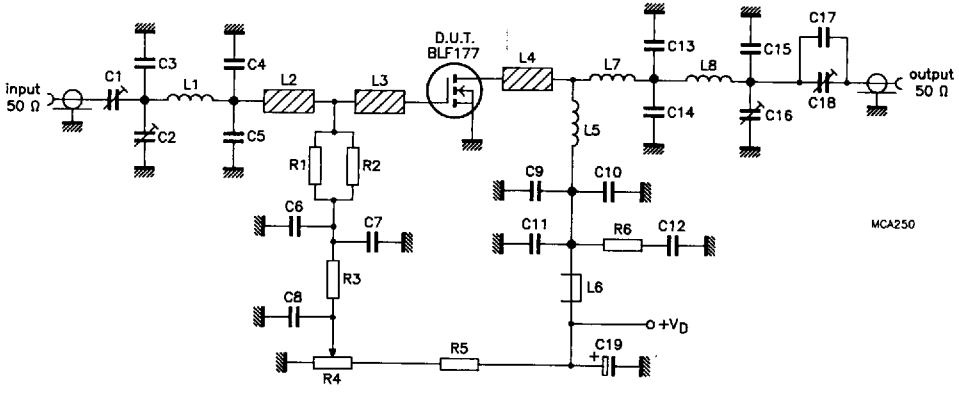
Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 mA; R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.17 Two tone efficiency as a function of load power, typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 A; R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.18 Load power as a function of input power, typical values.



f = 108 MHz.

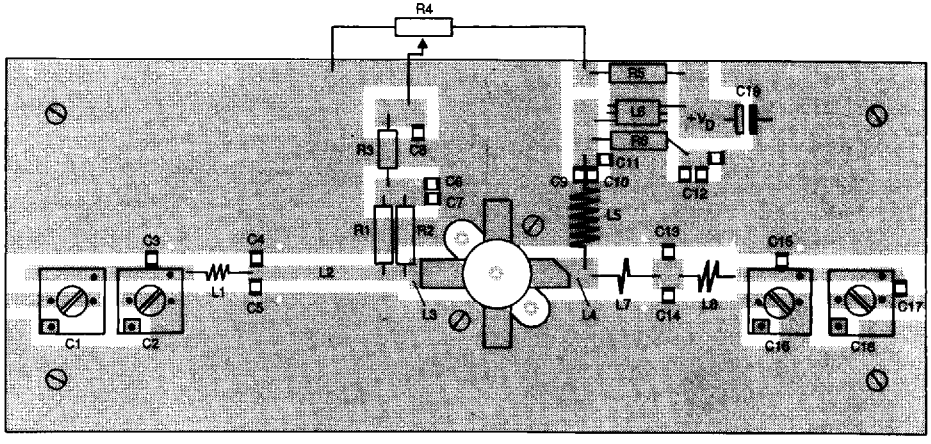
Fig.19 Test circuit for class-B operation.

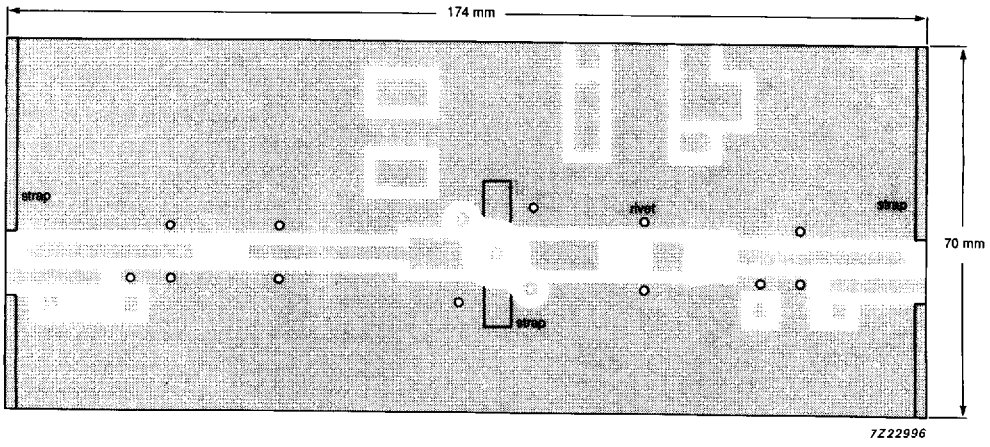
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C16, C18	film dielectric trimmer	2.5 to 20 pF		2222 809 07004
C3	multilayer ceramic chip capacitor (note 1)	20 pF		
C4, C5	multilayer ceramic chip capacitor (note 1)	62 pF		
C6, C7, C9, C10	multilayer ceramic chip capacitor (note 1)	1 nF		
C8	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C11	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C12	multilayer ceramic chip capacitor	3 x 100 nF		2222 852 47104
C13, C14	multilayer ceramic chip capacitor (note 1)	36 pF		
C15	multilayer ceramic chip capacitor (note 1)	12 pF		
C17	multilayer ceramic chip capacitor (note 1)	5.6 pF		
C19	electrolytic capacitor	4.4 µF, 63 V		2222 030 28478
L1	3 turns enamelled 0.8 mm copper wire	22 nH	length 5.5 mm; int. dia. 3 mm; leads 2 x 5 mm	
L2	stripline (note 2)	64.7 Ω	31 x 3 mm	
L3, L4	stripline (note 2)	41.1 Ω	10 x 6 mm	
L5	6 turns enamelled 1.6 mm copper wire	122 nH	length 13.8 mm; int. dia. 6 mm; leads 2 x 5 mm	
L6	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L7	1 turn enamelled 1.6 mm copper wire	16.5 nH	int. dia. 9 mm; leads 2 x 5 mm	
L8	2 turns enamelled 1.6 mm copper wire	34.4 nH	length 3.9 mm; int. dia. 6 mm; leads 2 x 5 mm	
R1, R2	1 W metal film resistor	31.6 Ω		
R3	0.4 W metal film resistor	1 kΩ		
R4	cermet potentiometer	5 kΩ		
R5	0.4 W metal film resistor	44.2 Ω		
R6	1 W metal film resistor	10 Ω		

Notes

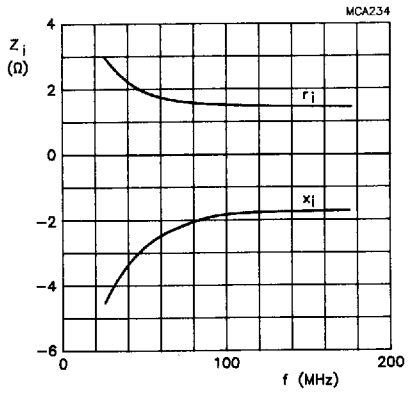
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$), thickness 1.6 mm.





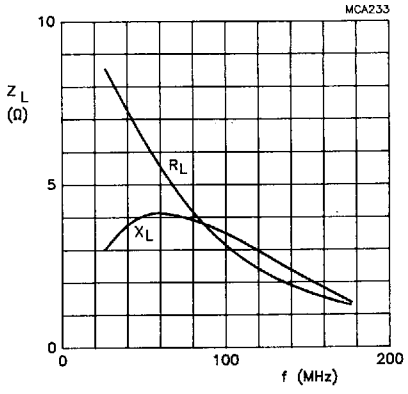
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the source leads and at the input and output copper straps are used for a direct contact between upper and lower sheets.

Fig.20 Component layout for 108 MHz class-B test circuit.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.21 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.22 Load impedance as a function of frequency (series components), typical values.

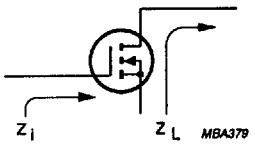
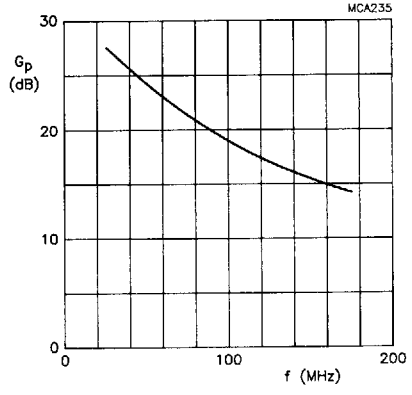


Fig.23 Definition of MOS impedance.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.24 Power gain as a function of frequency, typical values.