U.H.F. LINEAR POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor primarily intended for use in **linear u.h.f. amplifiers** for television transmitters and transposers. The **excellent d.c. dissipation properties** for class-A operation are obtained by means of diffused emitter ballasting resistors and a multi-base structure, providing an optimum temperature profile on the crystal area. The combination of optimum thermal design and the application of **gold sandwich metallization** realizes excellent reliability properties.

The transistor has a ¼" capstan envelope with ceramic cap.

QUICK REFERENCE DATA

R.F. performance

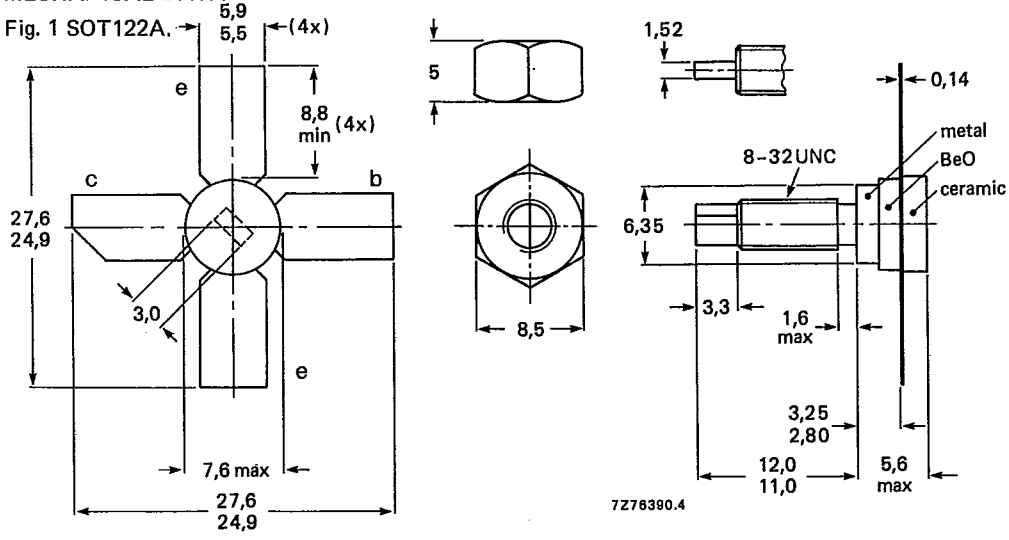
mode of operation	f_{vision} MHz	V_{CE} V	I_C mA	T_h °C	d_{im} * dB	$P_{o\ sync}$ * W	G_p dB
class-A; linear amplifier	860	25	150	70	−60	> 0,5	> 11
	860	25	150	25	−60	typ. 0,63	typ. 12,2

* Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT122A.



Torque on nut: min. 0,75 Nm (7,5 kg cm)
max. 0,85 Nm (8,5 kg cm)

Diameter of clearance hole in heatsink: max. 4,2 mm.
Mounting hole to have no burrs at either end.
De-burring must leave surface flat; do not chamfer or countersink either end of hole.

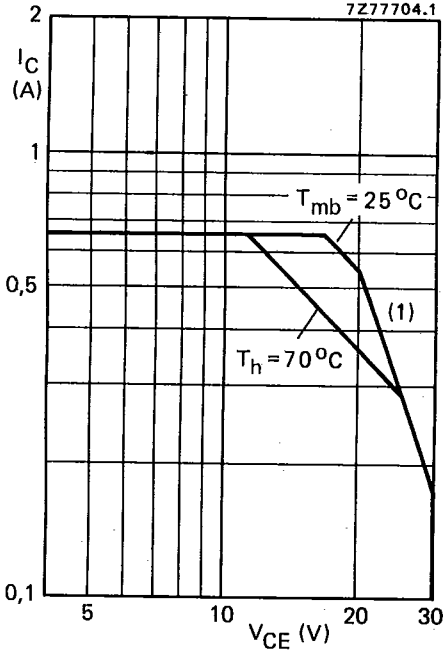
When locking is required an adhesive is preferred instead of a lock washer.

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage (peak value); $V_{BE} = 0$	V_{CESM}	max.	50 V
open base	V_{CEO}	max.	30 V
Emitter-base voltage (open collector)	V_{EBO}	max.	4 V
Collector current d.c. or average	I_C	max.	650 mA
(peak value); f > 1 MHz	I_{CM}	max.	1000 mA
Total power dissipation up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	10,8 W
Storage temperature	T_{stg}		−65 to +150 °C
Operating junction temperature	T_j	max.	200 °C



(1) Second breakdown limit (independent of temperature).

Fig. 2 D.C. SOAR.

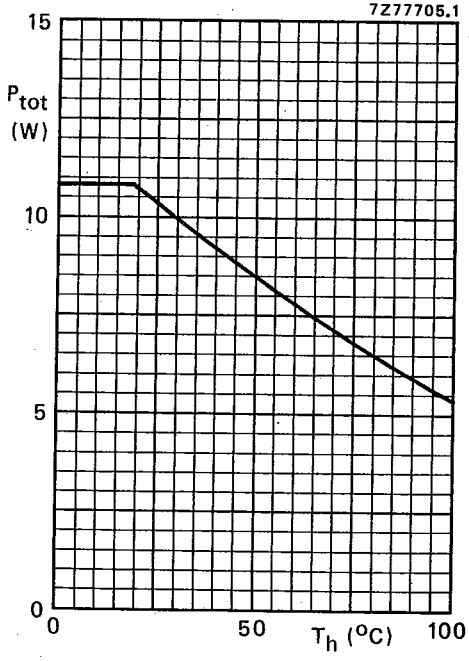


Fig. 3 Power derating curve vs. temperature.

THERMAL RESISTANCE (see Fig. 4)

From junction to mounting base (dissipation = 3,75 W; $T_{mb} = 72,3\ ^oC$; i.e. $T_h = 70\ ^oC$)	$R_{th\ j\text{-}mb}$	=	15,0 K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,6 K/W

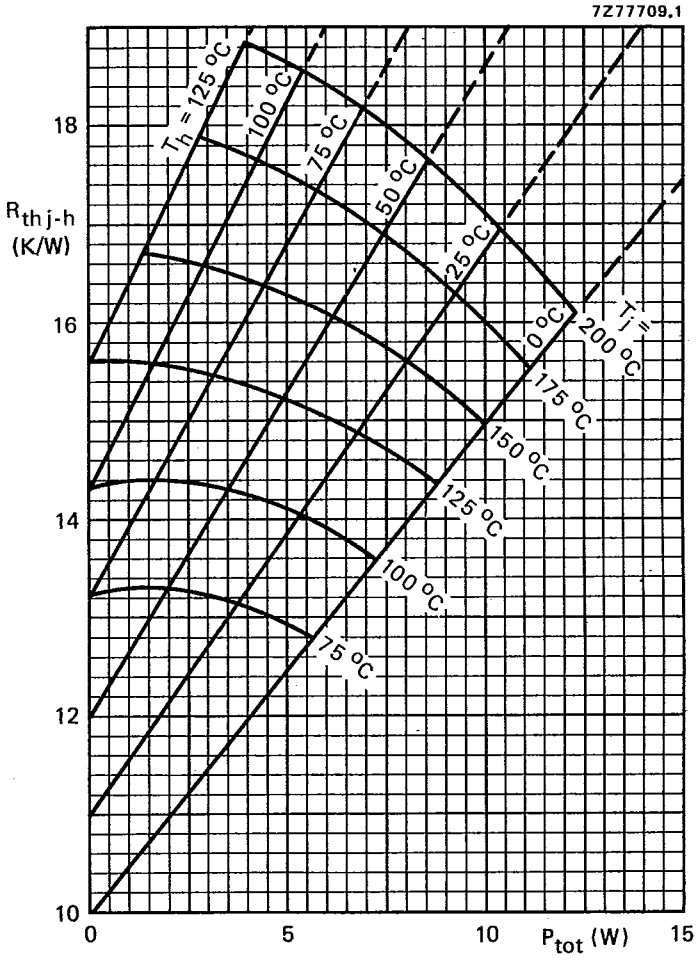


Fig. 4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters. ($R_{th\ mb\text{-}h}$ = 0,6 K/W.)

Example

Nominal class-A operation: V_{CE} = 25 V; I_C = 150 mA; T_h = 70 °C.

Fig. 4 shows:	$R_{th\ j\text{-}h}$	max.	15,6 K/W
	T_j	max.	130 °C
Typical device:	$R_{th\ j\text{-}h}$	typ.	13,5 K/W
	T_j	typ.	120 °C

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-emitter breakdown voltage			
V_{BE} = 0; I_C = 2 mA	$V_{(BR)CES}$	>	50 V
open base; I_C = 15 mA	$V_{(BR)CEO}$	>	30 V
Emitter-base breakdown voltage			
open collector; I_E = 1 mA	$V_{(BR)EBO}$	>	4 V
Collector cut-off current			
V_{BE} = 0; V_{CE} = 30 V	I_{CES}	<	0,5 mA
V_{BE} = 0; V_{CE} = 30 V; T_j = 175 °C	I_{CES}	<	1,2 mA
D.C. current gain *			
I_C = 150 mA; V_{CE} = 25 V	h_{FE}	>	20
		typ.	40
I_C = 150 mA; V_{CE} = 25 V; T_j = 175 °C	h_{FE}	<	120
Collector-emitter saturation voltage *			
I_C = 300 mA; I_B = 30 mA	V_{CEsat}	typ.	500 mV
Transition frequency at f = 500 MHz **			
$-I_E$ = 150 mA; V_{CB} = 25 V	f_T	typ.	3,5 GHz
$-I_E$ = 300 mA; V_{CB} = 25 V	f_T	typ.	3,4 GHz
Collector capacitance at f = 1 MHz			
$I_E = I_e$ = 0; V_{CB} = 25 V	C_c	typ.	3,7 pF
Feedback capacitance at f = 1 MHz			
I_C = 10 mA; V_{CE} = 25 V	C_{re}	typ.	1,9 pF
Collector-stud capacitance	C_{cs}	typ.	1,2 pF

* Measured under pulse conditions: $t_p \leqslant 300\ \mu s$; $\delta \leqslant 0{,}02$.

** Measured under pulse conditions: $t_p \leqslant 50\ \mu s$; $\delta \leqslant 0{,}01$.

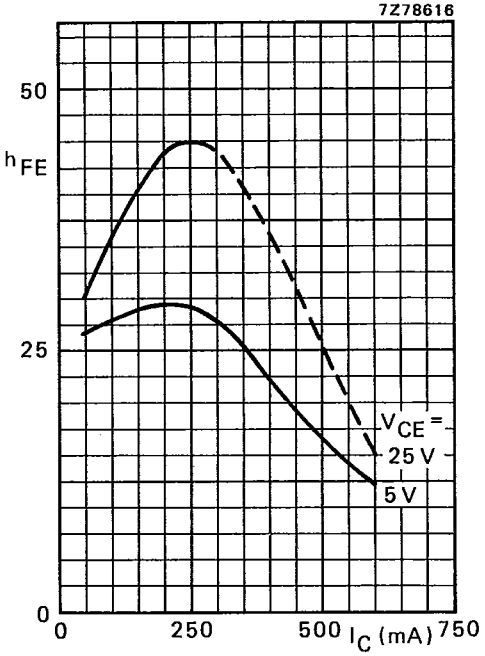


Fig. 5 Typical values; T_j = 25 °C.

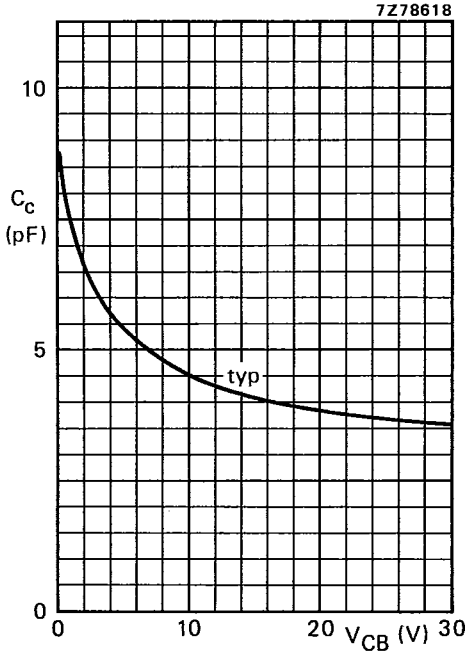


Fig. 6 $I_E = I_e = 0$; f = 1 MHz; T_j = 25 °C.

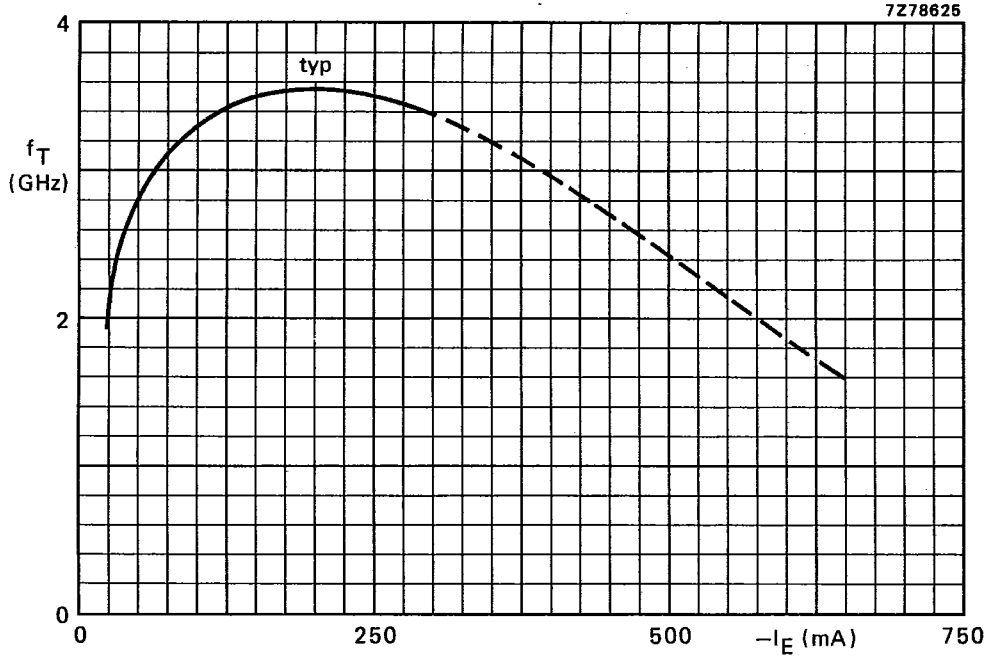


Fig. 7 V_{CB} = 25 V; f = 500 MHz; T_j = 25 °C.

APPLICATION INFORMATION

f_{vision} (MHz)	V_{CE} (V)	I_C (mA)	T_h (°C)	d_{im} (dB) *	$P_{o\,sync}$ (W) *	G_p (dB)
860	25	150	70	−60	> 0,5	> 11
860	25	150	70	−60	typ. 0,58	typ. 12,2
860	25	150	25	−60	typ. 0,63	typ. 12,2

* Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

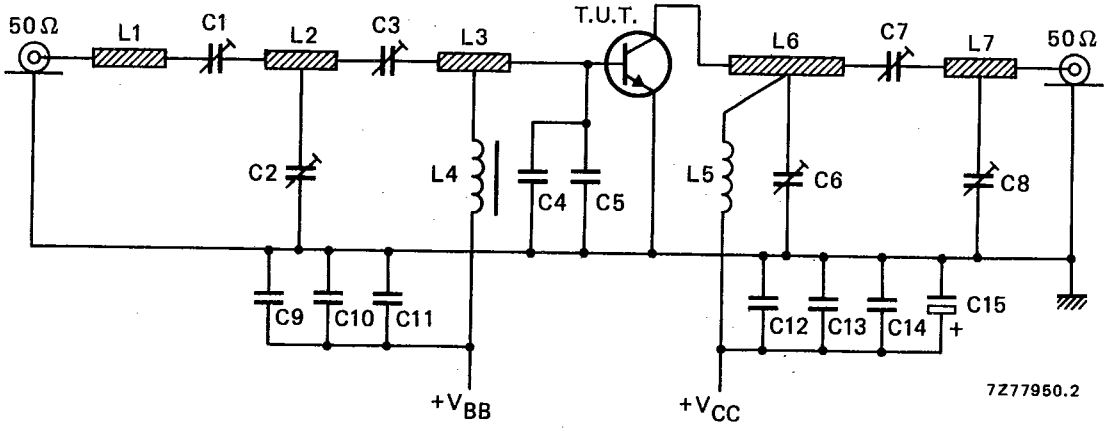


Fig. 8 Test circuit at f_{vision} = 860 MHz.

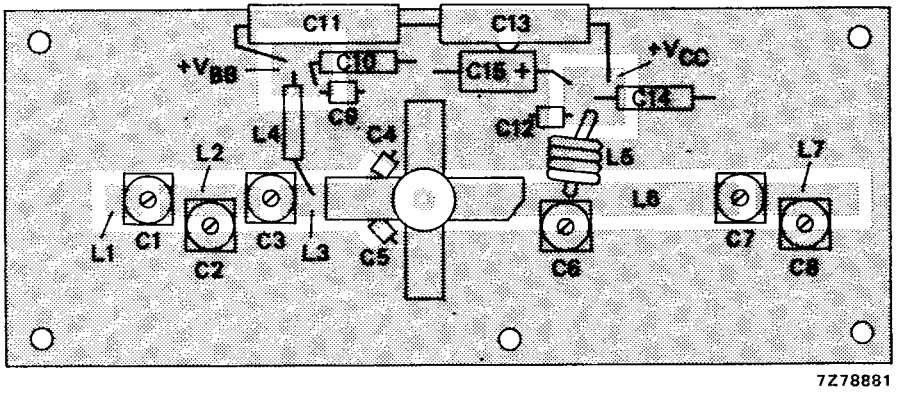
List of components:

C1 = C7 = 2 to 18 pF film dielectric trimmer (cat. no. 2222 809 05003)
C2 = C6 = C8 = 1 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001) placed 24 mm, 17 mm and 45 mm respectively from transistor edge
C3 = 1,8 to 10 pF film dielectric trimmer (cat. no. 2222 809 05002)
C4 = C5 = 3 pF multilayer chip capacitor (ATC 100A-3RO-C-PX-50)
C9 = C12 = 1 nF chip capacitor
C10 = 100 nF polyester capacitor
C11 = C13 = 470 nF polyester capacitor
C14 = 10 nF polyester capacitor
C15 = 3,3 μF/40 V solid aluminium electrolytic capacitor

L1 = stripline (5,0 mm x 4,5 mm)
L2 = stripline (13,2 mm x 4,5 mm)
L3 = stripline (15,0 mm x 4,5 mm)
L4 = micro choke 0,47 μH (cat. no. 4322 057 04770)
L5 = 4 turns closely wound enamelled Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2 x 4 mm
L6 = stripline (37,0 mm x 4,5 mm)
L7 = stripline (13,5 mm x 4,5 mm)

L1; L2; L3; L6 and L7 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric (ϵ_r = 2,74); thickness 1/16".

Component layout and printed-circuit board for 860 MHz test circuit are shown in Fig. 9. For bias circuit see Fig. 10.



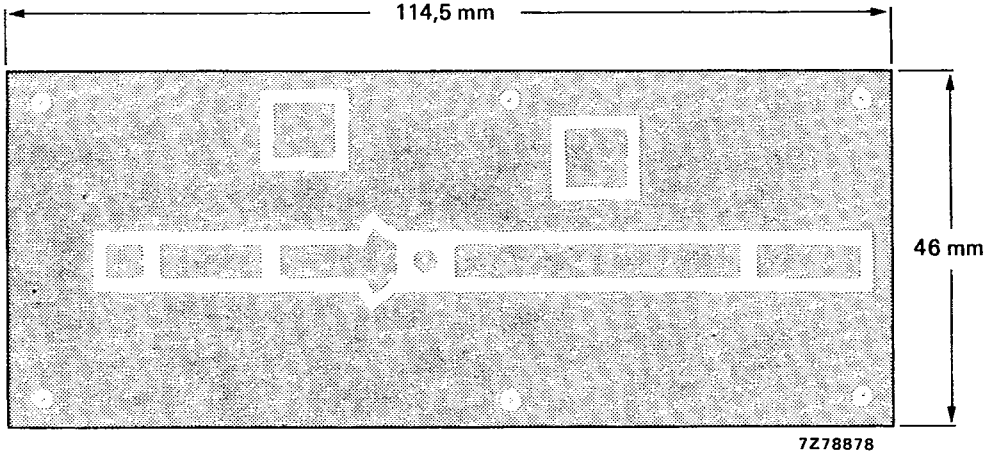
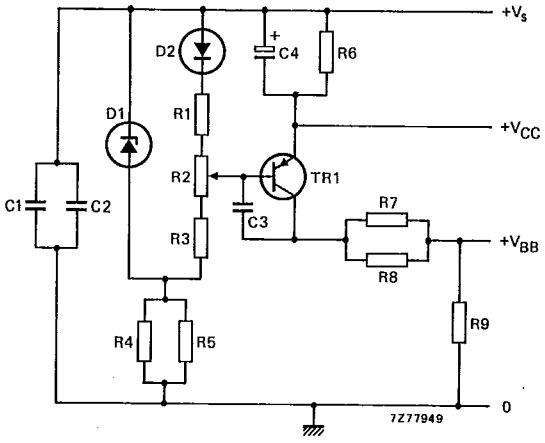


Fig. 9 Component layout and printed-circuit board for 860 MHz test circuit.

The circuit and the components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.



List of components:

C1 = 100 pF ceramic capacitor
C2 = C3 = 100 nF polyester capacitor
C4 = 10 μF/25 V solid aluminium electrolytic capacitor
R1 = 150 Ω carbon resistor (0,25 W)
R2 = 100 Ω preset potentiometer (0,1 W)
R3 = 82 Ω carbon resistor (0,25 W)
R4 = R5 = 2,2 kΩ carbon resistor (0,25 W)
R6 = 12 Ω carbon resistor (0,5 W)
R7 = R8 = 820 Ω carbon resistor (0,25 W)
R9 = 33 Ω carbon resistor (0,25 W)

D1 = BZY88-C3V3
D2 = BY206
TR1 = BD136

Fig. 10 Bias circuit for class-A amplifier at f_{vision} = 860 MHz.

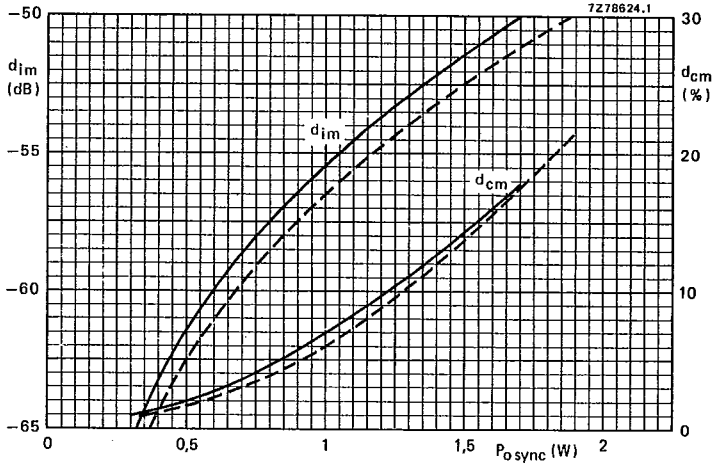


Fig. 11 Intermodulation distortion (d_{im})* and cross-modulation distortion (d_{cm})** as a function of output power. Typical values; V_{CE} = 25 V; I_C = 150 mA; f_{vision} = 860 MHz; –––– T_h = 25 °C; —— T_h = 70 °C.

Information for wideband application from 470 to 860 MHz available on request.

* Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.
Intermodulation distortion of input signal ⩽ −75 dB.

** Two-tone test method (vision carrier 0 dB, sound carrier −7 dB), zero dB corresponds to peak sync level.
Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to −20 dB.

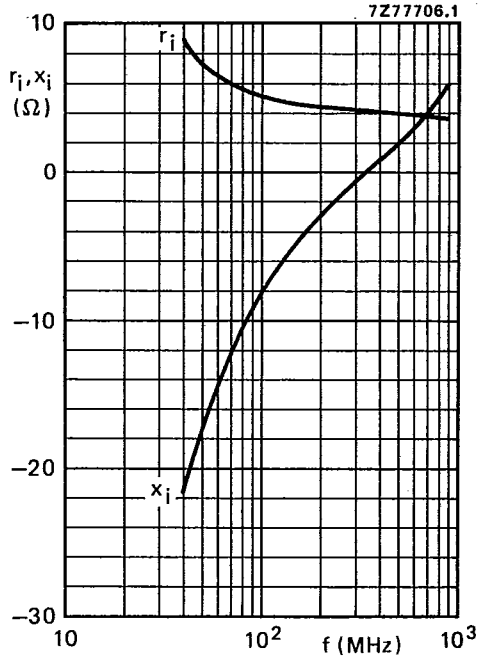


Fig. 12 Input impedance (series components).

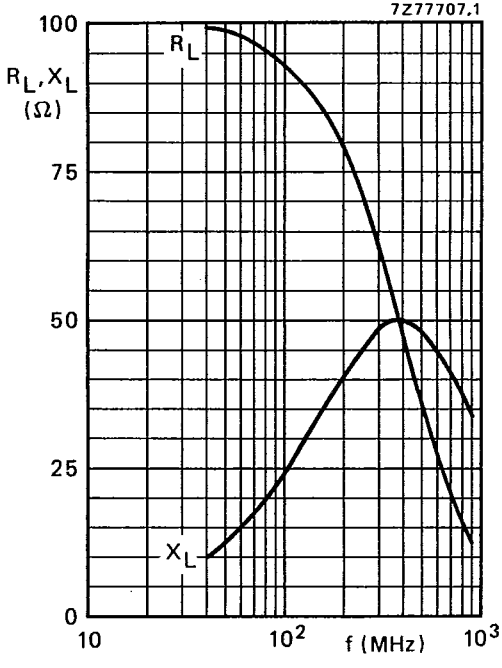


Fig. 13 Load impedance (series components).

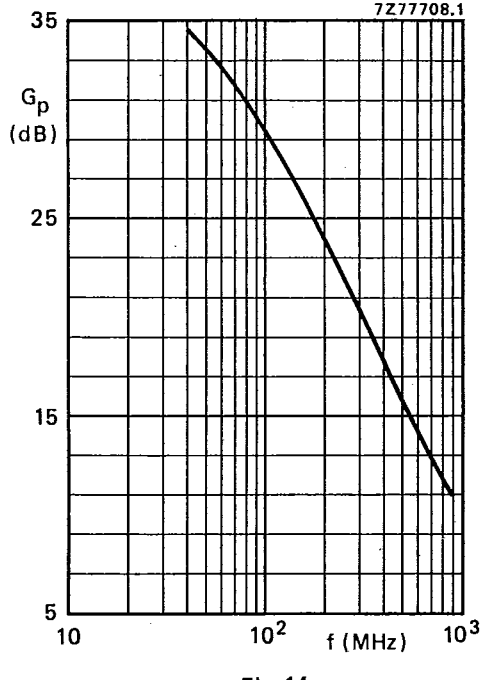


Fig. 14.

Conditions for Figs 12, 13 and 14:

Typical values; V_{CE} = 25 V; I_C = 150 mA; T_h = 70 °C.

Ruggedness

The BLW32 is capable of withstanding a load mismatch (VSWR = 50 through all phases) under the following conditions:

f = 860 MHz; V_{CE} = 25 V; I_C = 150 mA; T_h = 70 °C and P_L = 1 W.